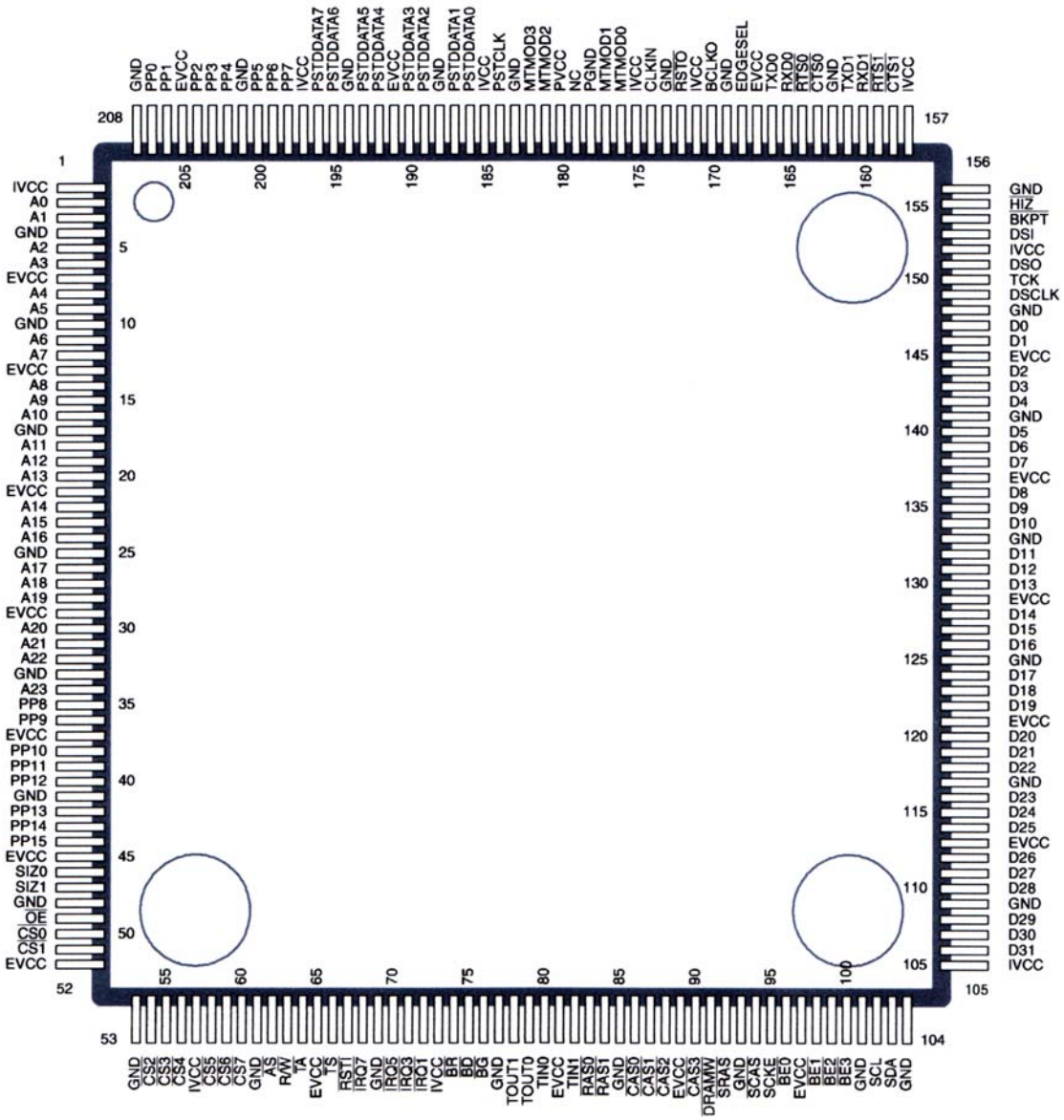
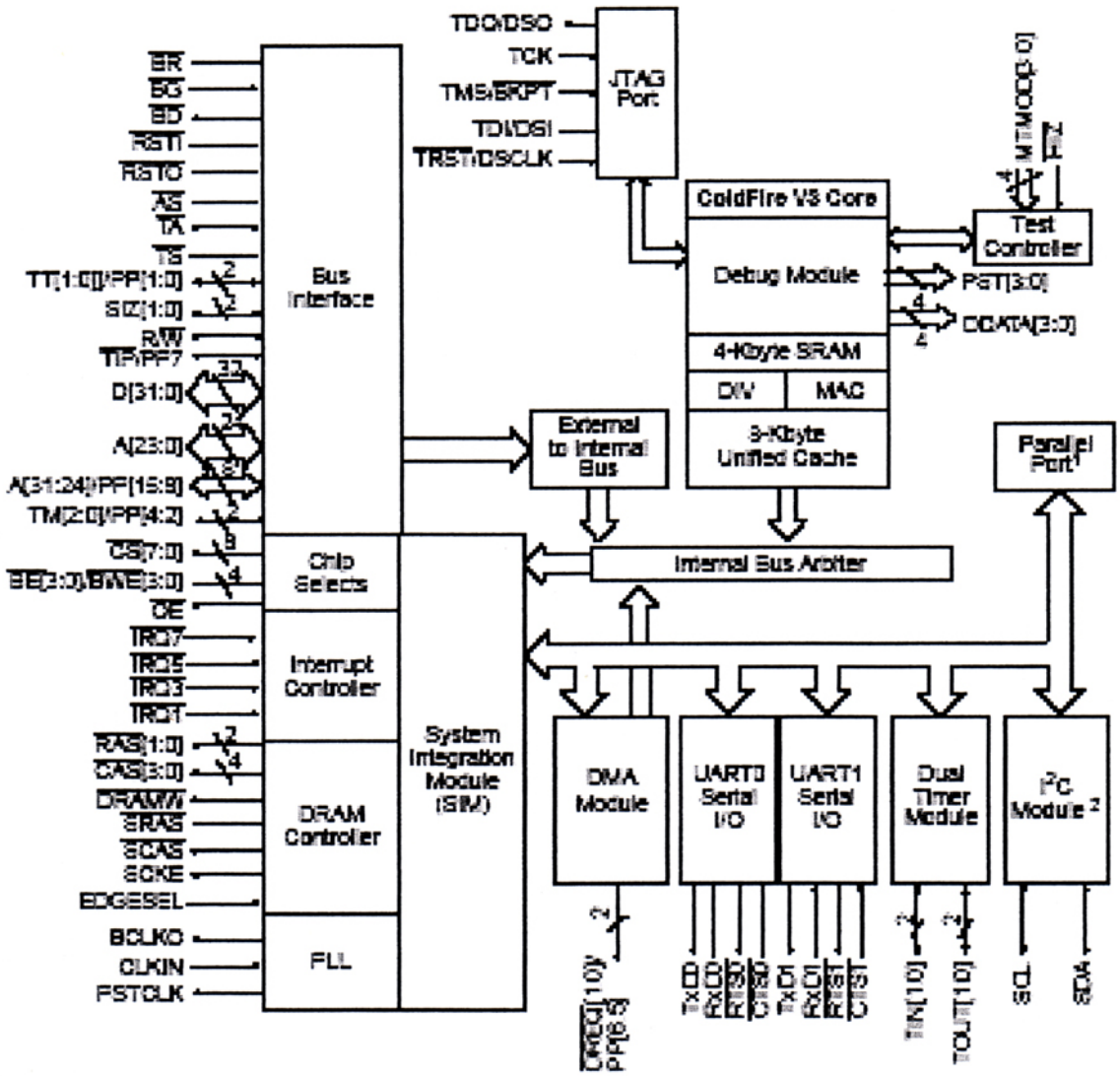
6.1 - brochage du composant MCF5307.

Brochage 5307 == 5407. Ici Brochage du 5407 avec les broches IVCC @1,8 volts.
Ces broches sont à 3,3 Volts dans la version 5307.



Mechanical Diagram

6.2 - Brochage fonctionnel associé



[1] Note: Parallel port pins (PPn) are multiplexed with other bus functions as shown.
[2] I2C is a Philips proprietary interface

7.1 - Mapping des registres qui n'appartiennent pas au modèle de programmation

Table B-1. SIM Registers

MBAR offset	[31:24]	[23:16]	[15:8]	[7:0]
0x000	Reset status register (RSR)	System protection control register (SYPCR)I	Software watchdog interrupt vector register (SWIVR)	Software watchdog service register (SWSR)
0x004	Pin assignment register (PAR)		Interrupt port assignment register (IRQPAR)	Reserved
0x008	PILL control (PLLCR)	Reserved		
0X00C	Default bus master park register (MPARK)	Reserved		
0X010 - 0x03C	Reserved			

Table B-2. Interrupt Controller Registers

MBAR offset	[31:241	[23:16]	[15:8]	[7:0]
Interrupt Registers				
0x040	Interrupt pending register (IPR)			
0x044	Interrupt mask register IMR			
0x048	Reserved			Autovector register (AVR)
Interrupt Control Registers (ICRs)				
0x04C	Software watchdog timer (ICR0)	Timer 0 (ICR1)	Timer 1 (ICR2)	12C (ICR3)
0x050	UART0 (ICR4)	UART1 (ICR5)	DMA0 (ICR6)	DMA1 (ICR7)
0x054	DMA2 (ICR8)	DIVIA3 (ICR9)	Reserved	

Table B3 -Chip-select registers

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0X080	Chip-select address register-bank 0 (CSAR0)		Reserved	
0x084	Chip-select mask register-bank 0 (CSMR0)			
0x088	Reserved		Chip-select control register-bank 0 (CSCR0)	
0x08C	Chip-select address register-bank 1 (CSARI)		Reserved	
0X090	Chip-select mask register-bank 1 (CSMR1)			
0x094	Reserved		Chip-select control register-bank I (CSCR1)	
0x098	Chip-select address register-bank 2 (CSAR2)		Reserved	
0X09C	Chip-select mask register--bank 2 (CSMR2)			
0x0A0	Reserved		Chip-select control register--bank 2 (CSCR2)	
0x0A4	Chip-select address register-bank 3 (CSAR3)		Reserved	
0x0A8	Chip-select mask register-bank 3 (CSMR3)			
0x0AC	Reserved		Chip-select control register-bank 3 (CSCR3)	
0x0B0	Chip-select address register-bank 4 (CSAR4)		Reserved'	
0x0B4	Chip-select mask register-bank 4 (CSMR4)			
0x0B8	Reserved		Chip-select control register-bank 4 (CSCR4)	
0x0BC	Chip-select address register-bank 5 (CSAR5)		Reservedl	
0xDC0	Chip-select mask register-bank 5 (CSMR5)			
0x0C4	Reserved		Chip-select control register-bank 5 (CSCR5)	
0x0C8	Chip-select address register--bank 6 (CSAR6)		Reserved'	
0X0CC	Chip-select mask register-bank 6 (CSMR6)			
0x0D0	Reserved		Chip-select control register-bank 6 (CSCR6)	
0x0D4	Chip-select address register-bank 7 (CSAR7)		Reserved'	
0x0D8	Chip-select mask register-bank 7 (CSMR7)			
0x0DC	Reserved		Chip-select control register-bank 7 (CSCR7)	

Table B-3. –Chip-Select Registers, (Continued)

MBAR Offset	[31:24]	123:16]	[15:8]	[7:0]
MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0X080	Chip-select address register-bank 0 (CSAR0)		Reserved	
0x084	Chip-select mask register--bank 0 (CSMR0)			
0x088	Reserved		Chip-select control register-bank 0 (CSCR0)	
0x08C	Chip-select address register-bank 1 (CSAR1)		Reserved	
0X090	Chip-select mask register-bank 1 (CSMR1)			
0x094	Reserved		Chip-select control register-bank 1 (CSCR1)	
0x098	Chip-select address register-bank 2 (CSAR2)		Reserved	
0X09C	Chip-select mask register-bank 2 (CSMR2)			
0x0A0	Reserved		Chip-select control register-bank 2 (CSCR2)	
0x0A4	Chip-select address register-bank 3 (CSAR3)		Reserved	
0x0A8	Chip-select mask register-bank 3 (CSMR3)			
0x0AC	Reserved		Chip-select control register-bank 3 (CSCR3)	
0x0B0	Chip-select address register-bank 4 (CSAR4)		Reserved	
0x0B4	Chip-select mask register-bank 4 (CSMR4)			
0x0B8	Reserved		Chip-select control register--bank 4 (CSCR4)	

Table B-4. DRAM Controller Registers

MBAR Offset	[31:241	123:161	[15:81	[7:0]
0X100	DRAM control register (DCR)		Reserved	
0x104	Reserved			
0x108	DRAM address and control register 0 (DACR0)			
0X10C	DRAM mask register block 0 (DM R0)			
0X110	DRAM address and control register 1 (DACR1)			
0x114	DRAM mask register block 1 (DMR1)			

Table B-5. General-Purpose Timer Registers

MBAR offset	[31:24	123:16]	[15:8]	[7:0]
0x140	Timer 0 mode register (TIVIR0) [p. 13-3]		Reserved	
0x144	Timer 0 reference register (TRR0) [p. 13-4]		Reserved	
0x148	Timer 0 capture register (TCR0) [p. 13-4]		Reserved	
0x14C	Timer 0 counter (TCN0) [p. 13-5]		Reserved	
0x150	Reserved Timer 0 event register (TER0)		Reserved	
0x180	Timer 1 mode register (TIVIR1) [p. 13-3]		Reserved	
0x184	Timer 1 reference register (TRR1) [p. 13-4]		Reserved	
0x188	Timer 1 capture register (TCR1) [p. 13-4]		Reserved	
0x18C	Timer 1 counter (TCN1) [p. 13-5]		Reserved	
0X190	Reserved Timer 1 event register		Reserved	

Table B-6. UART0 Control Registers

MBAR Offset	[31:24]	[23:16]	[15:8]	17:01
UART0 Control Registers				
0X1C0	UART mode registers' (UM R1 n) , (UMR2n)			
0x1C4	(Read) UART status registers-(USRn)			
	(Write) UART clock-select register'-(UCSRn)			
0x1C8	(Read) Do not access2 -			
	(Write) UART command -registers,-(UCRn)			
0X1CC	(Read) UART receiver - buffers--(URBn)			
	(Write) UART transmitter -buffers--(UTBn)]			

Table B-6. UART0 Control Registers (Continued)

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:01
0x1D0	(Read) UART input port - change registers-(UIPCRn)			
	(Write) UART auxiliary -control registersl--(UACRn)			
0x1D4	(Read) UART interrupt - status registers-(UISRn)			
	(Write) UART interrupt -mask registers-(UIMRn)			
0x1D8	UART divider upper registers-(UDUn)			
0x1DC	UART divider lower registers-(UDLn)			
0x1E0 0x1EC	Do not acoess2			
0x1F0	UART interrupt vector register--(UIVRn)			
0x1F4	(Read) UART input port registers-(UlPn)			
	(Write) Do not access			
0x1F8	(Read) Do not access 2 -			
	(Write) UART output port bit set command registers-(U0P10)			
0x1FC	(Read) Do not access 2 -			
	(Write) UART output port bit reset command registers-(U0P0n3)			

1 UIVIR1 n, UIVIR2n, UCSRn, and UACRn[BRG] should be changed only after the receiver/transmitter is issued a software reset command. That is, if channel operation is not disabled, undesirable results may occur.

2 This address is for factory testing. Reading this location results in undesired effects and possible incorrect transmission or reception of characters. Register contents may also be changed.

Table B-7. UART1 Control Registers

MBAR offset	[31:241	[23:16]	[15:8]	[7:0]
UAFTT1 Control Registers				
0x200	UART mode registers'--(UMR1 n), (LIMR2n)	Rx FIFO threshold register-(RXLVL)	Modem control register--(MODCTL)	Tx FIFO threshold register--(TXLVL)
0x204	(Read) UART status registers-(USRn)	-	(Read) Rx samples available register--(RSMP)	(Read) Tx space available register-(TSPC)
	(Write) UART clock-select register-(UCSRn)			
0x208	(Read) Do not access[2]			
	(Write) UART command - registers-(UCRn)			
0x20C	(Read) UART receiver buffers--(URBn)			
	(Write) UART transmitter buffers--(UTBn)			
0x2l 0	(Read) UART input port -change registers-(UIPCRn)			
	(Write) UART auxiliary -control registersl--(UACRn)			
0x214	(Read) UART interrupt status registers-(UISRn)			
	(Write) UART interrupt -mask registers-(UIMRn)			
0x218	UART divider upper registers-(UDUn)			
0x21C	UART divider lower registers-(UDLn)			
Ox220-Ox22C	Do not access2			

Table B-7. UART1 Control Registers (Continued)

MBAR offset	[31:24]	[23:16]	[5:8]	[7:0]
0x230	UART interrupt vector register--(UIVRn)			
0x234	(Read) UART input port registers-(UlPn)			
	(Write) Do not access			
0x238	(Read) Do not access			
	(Write) UART output port bit set command registers-(UOPln3)			
0x23C	(Read) Do not access 2			
	(Write) UART output port bit reset command registers-(UOPon3)			
0x200	UART mode registeM4--(UMRln) , (UMR2n)	Rx FIFO threshold register-(RXLVL) (UART1 only)	Modem control register--(MODCTL) (UART1 only)	Tx FIFO threshold register--(TXLVL) (UART1 only)
0x204	(Read) UART status registerr,--(USRn)			
	(Write) UART clock-select register'-(UCSRn)			

1 UMR1 n, UMR2n, UCSRn, and UACRn[BRG] should be changed only after the receiver/transmitter is issued a software reset command. That is, if channel operation is not disabled, undesirable results may occur.

2 This address is for factory testing. Reading this location results in undesired effects and possible incorrect transmission or reception of characters. Register contents may also be changed.

3 Address-triggered commands

4 UMR1 n, UMR2n, UCSRn, and UACRn[BRG] should be changed only after the receiver/transmitter is issued a software reset command. That is, if channel operation is not disabled, undesirable results may occur.

Table B-8. Parallel Port Memory Map

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x244	Parallel port data direction register (PADDR)		Reserved	
0x248	Parallel port data register (PADAT)		Reserved	

Table B-9. I²C Interface Memory Map

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x280	1² C address register (IADR)	Reserved		
0x284	1²C frequency divider register (IFDR)	Reserved		
0x288	1²C control register (12CR)	Reserved		
0x28C	1²C status register (I2SR)	Reserved		
0x290	1²C data I/0 register (I2DR)	Reserved		

Table B-10. DMA Controller Registers

MBAR offset	[31:24]	[23:16]	[15:8]	[7:0]
0X300	Source address register 0 (SAR0)			
0x304	Destination address register 0 (DAR0)			
0x308	DMA control register 0 (DCR0)			
0x30C	Reserved	Byte count register 0 (BCR0)		
0x310	DMA status register 0 (DSR0)	Reserved		
0x314	DMA interrupt vector register 0 (DSR0)	Reserved		
0x340	Source address register I (SAR1)			
0x344 I	Destination address register 1 (DAR1)			
0x348	DMA control register 1 (DCR1)			
0x34C	Reserved	Byte count register 1 (BCR1)		
0x350	DMA status register 1 (DSR1)	Reserved		
0x354	DMA interrupt vector register 1 (DSR1)	Reserved		
0x380	Source address register 2 (SAR2)			
0x384	Destination address register 2 (DAR2)			
0x388	DMA control register 2 (DCR2)			
0x38C	Reserved	Byte count register 2 (BCR2)		
0X390	DMA status register 2 (DSR2)	Reserved		

Table B-10. DMA Controller Registers (Continued)

MBAR Offset	[31:24]	[23:16]	115:8]	[7:01
0X394	DMA interrupt vector register 2 (DIVR2)	Reserved		
0x3C0	Source address register 3 (SAR3)			
0x3C4	Destination address register 3 (DAR3)			
0x3C8	DMA control register 3 (DCR3)			
0x3CC	Reserved	Byte count register 3 (BCR3)		
0x3D0	DMA status register 3 (DSR3)	Reserved		
0x3D4	DMA interrupt vector register 3 (DIVR3)	Reserved		